

1 Code Analysis

Given the follow chunk of code, analyze the hit rate given that we have a byte-addressed computer with a total memory of 1 MiB. It also features a 16 KiB Direct-Mapped cache with 1 KiB blocks.

```
#define NUM_INTS 8192 // 2^13
int A[NUM_INTS]; // A lives at 0x10000
int i, total = 0;
for (i = 0; i < NUM_INTS; i += 128) {
    A[i] = i; // Line 1
}
for (i = 0; i < NUM_INTS; i += 128) {
    total += A[i]; // Line 2
}
```

- 1.1 How many bits make up a memory address on this computer?

$$1 \text{ MiB} = 2^{20} \text{ B} \rightarrow \log 2^{20} = \underline{20 \text{ bits}} \quad T: 20 - 10 - 4 = 6 \text{ bits}$$

- 1.2 What is the T:I:O breakdown?

$$O: 1 \text{ KiB} = 2^{10} \text{ B} \rightarrow \log 2^{10} = 10 \text{ bits} \quad I: \frac{16 \text{ KiB}}{1 \text{ KiB}} = 16 \text{ indices} \rightarrow \log 16 = 4 \text{ bits}$$

- 1.3 Calculate the cache hit rate for the line marked Line 1:

jumping $4 \cdot 128 = 512 \text{ B}$ each loop
 $\rightarrow 2 \text{ elems fit in each block} \Rightarrow A[i] \text{ pulls in } A[i+128] \Rightarrow 50\% \text{ HR}$



- 1.4 Calculate the cache hit rate for the line marked Line 2:

array size = $2^{13} \cdot 4 = 2^{15} \text{ B} \rightarrow \text{twice as big as cache!}$
 $\rightarrow \text{cannot fit inside} \rightarrow 50\% \text{ HR for reason above.}$

2 AMAT

Recall that AMAT stands for Average Memory Access Time. The main formula for it is:

$$\text{AMAT} = \text{Hit Time} + \text{Miss Rate} * \text{Miss Penalty}$$

We also have two types of miss rates, global and local. Global is calculated as: Fraction of ALL accesses that missed at that level over all accesses total. Whereas local is calculated: Fraction of ALL access that missed at that level over all access to that level total.

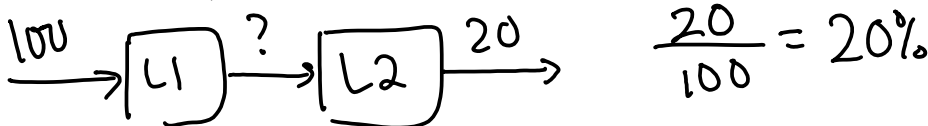
Note L_1 global = local



$$G = \frac{\text{Misses Here}}{\text{Total Access}}$$

$$L = \frac{\text{Misses Here}}{\text{Accesses Here}}$$

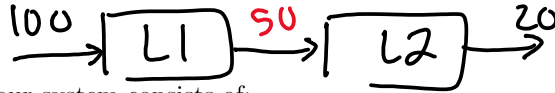
- 2.1 An L2\$, out of 100 total accesses to the cache system, missed 20 times. What is the global miss rate of L2\$?



↖ L1 miss rate

$$100 \cdot MR = 100 \cdot 50\% = 50$$

2.2 If L1\$ had a miss rate of 50%, what is the local miss rate of L2\$?



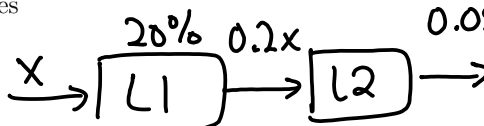
$$\frac{20}{50} = 40\%$$

Suppose your system consists of:

1. An L1\$ that hits in 2 cycles and has a local miss rate of 20%
2. An L2\$ that hits in 15 cycles and has a global miss rate of 5%
3. Main memory hits in 100 cycles

notice Local MR = $\frac{\text{Global MR}}{\text{L1 MR}}$

2.3 What is the local miss rate of L2\$?



$$LMR = \frac{0.05x}{.2x} = \frac{.05}{.2} = .25 = 25\%$$

2.4 What is the AMAT of the system?

2 ways

① using GMR: $2 + 20\% \cdot 15 + 5\% \cdot 100 = 2 + 3 + 5 = 10$ cycles

② using LMR: $2 + 20\% (15 + 25\% \cdot 100)$

L1 GMR, L2 GMR, L1 Hit time, L2 hit time, main mem ht

2.5 Suppose we want to reduce the AMAT of the system to 8 cycles or lower by adding in a L3\$. If the L3\$ has a local miss rate of 30%, what is the largest hit time that the L3\$ can have?

$$2 + 20\% (15 + 25\% \cdot (H + 30\% \cdot 100)) \leq 8$$

$$H = 30 \text{ cycles}$$

3 Floating Point

The IEEE 754 standard defines a binary representation for floating point values using three fields:

- The *sign* determines the sign of the number (0 for positive, 1 for negative)
- The *exponent* is in **biased notation** with a bias of 127
- The *significand* or *mantissa* is akin to unsigned, but used to store a fraction instead of an integer

The below table shows the bit breakdown for the single precision (32-bit) representation.

1	8	23
Sign	Exponent	Mantissa/Significand/Fraction

For normalized floats:

$$\text{Value} = (-1)^{\text{Sign}} * 2^{\text{Exp}-\text{Bias}} * 1.\text{significand}_2$$

For denormalized floats:

$$\text{Value} = (-1)^{\text{Sign}} * 2^{\text{Exp}-\text{Bias}+1} * 0.\text{significand}_2$$

Exponent	Significand	Meaning
0	Anything	Denorm
1-254	Anything	Normal
255	0	Infinity
255	Nonzero	NaN

↖ Write this on your cheat sheet!

forgetting denorm or ∞ on a test question... feels bad man.

3.1 How many zeroes can be represented using a float?

$$\begin{aligned} 100\dots 0 &\rightarrow -0 \\ 000\dots 0 &\rightarrow +0 \end{aligned}$$

2

3.2 What is the largest finite positive value that can be stored using a single precision float?

011...1 = NaN ⇒ not finite num
 ⇒ 011111110111...1 = 0x7FFFFFFF
 in decimal: $(2 - 2^{-23}) \cdot 2^{127}$

1.1111...1 = $2 - 2^{-23}$
 ↑ ↑ ↑
 $2^{-1} 2^{-2} \quad 2^{-23}$

3.3 What is the smallest positive value that can be stored using a single precision float?

00...01 = 0x00000001
 in decimal: $2^{-23} \cdot 2^{-126}$

denorm 0. ... 01
 ↑
 2^{-23}

3.4 What is the smallest positive normalized value that can be stored using a single precision float?

0000000100...0 = 0x00800000
 in decimal: $1 \cdot 2^{-126} = 2^{-126}$

3.5 Cover the following numbers from binary to decimal or from decimal to binary:

- 0x00000000 = 0
- 39.5625
- 8.25 ①
- 0xFF94BEEF
- 0x00000F00 ② 4 0's
- -∞ ③

① 1000.01 = 1,00001 × 2³
 exp = 3 + 127 = 130
 ⇒ 0100000100000100...0
 = 0x41040000

denorm!
 0000 0000 0000 0000 1111 0000 0000
 4 Extra Stuff on Caches!

② 1.00...01111 · 2⁻¹²⁶ = $(2^{-12} + 2^{-13} + 2^{-14} + 2^{-15}) \cdot 2^{-126}$

③ 11111111 00...0
 ↑ neg ∞ 0s
 = 0xFF800000

4.1 Heres some practice involving a 2-way set associative cache. This time we have an 8-bit address space, 8 B blocks, and a cache size of 32 B. Classify each of the following accesses as a cache hit (H), cache miss (M) or cache miss with replacement (R). For any misses, list out which type of miss it is.

Address	T/I/O	Hit, Miss, Replace
0b0000 0100	0 0 4	M Comp
0b0000 0101	0 0 5	H
0b0110 1000	6 1 0	M Comp
0b1100 1000	12 1 0	M Comp
0b0110 1000	6 1 0	H
0b1101 1101	13 1 5	R Comp
0b0100 0101	4 0 5	M Comp
0b0000 0100	0 0 4	H
0b1100 1000	12 1 0	R, Capacity

4.2 What is the hit rate of our above accesses?

always draw your cache! index

O: $\log 8 = 3$ bits
 I: Blocks in cache = $\frac{32}{8} = 4$
 2 ways ⇒ $\frac{4}{2} = 2 \Rightarrow \log 2 = 1$ bit
 T = 8 - 3 - 1 = 4 bits

	way 1	valid	way 2	valid
Tag	data		data	
0	~	1	4	0
6	~	1	12 13 12	1